IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	December 9, 2008
Kubo, et al	Group Art Unit: 2621
Serial No. 10/716,791	Examiner: David Werner
Filed: November 19, 2003	IBM Corporation Anne Vachon Dougherty
Title: FORMAT CONVERSION CIRCUIT	3173 Cedar Road Yorktown Hts, NY 10598

Board of Patent Appeals and Interferences
Alexandria, VA 22313-1450

APPEAL BRIEF (37 CFR 41.37)

Appellants hereby appeal to the Board of Patent Appeals and Interferences from the decision dated July 9, 2008 of the Examiner finally rejecting Claims 1-7 in the above-identified patent application, and respectfully request that the Board of Patent Appeals and Interferences consider the arguments presented herein and reverse the Examiner's rejection.

I. REAL PARTY IN INTEREST

The appeal is made on behalf of Assignee, International Business Machines Corporation, the real party in interest with respect to the subject patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no pending related appeals or interferences with respect to the subject patent application.

III. STATUS OF CLAIMS

There are seven (7) claims pending in the subject patent application, numbered 1-7. No claims stand allowed. A complete copy of the claims involved in the appeal is attached hereto.

IV. STATUS OF AMENDMENTS

There are no unentered amendments filed after final rejection for the application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claims 1, 6 and 7

Independent Claims 1, 6 and 7 recite a formal conversion circuit (Claim 1), a format conversion method (Claim 6), and a computer readable storage device encoded with a computer program to perform a format conversion method (Claim 7). The claims recite format conversion steps and means (100 of Fig. 8) for conversion of digitized video data comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, including a memory and steps for storing video data (FIFO 101 of Fig. 8 and page 11, lines 14-20), header generation device and steps for generating a packet header that adheres to a standard for motion picture compression (Header

generation circuit 102 of Fig. 8 and page 11, lines 21-24), synchronous timing detector and steps for detecting a synchronizing signal for a line of video data (Circuit 103 of Fig. 8 and page 11, lines 25-29) and a selection device (counter 104 and switch 105 and page 11, line 30-page 12, line 23) and steps for repeating the selection of the packet header generated by said header generation means and selection of a predetermined amount of video data read out of said memory (page 14, lines 1-10) as a payload responsive to the packet header, during an interval from when said synchronous timing detection device detects the synchronizing signal for the line of data until it detects the next synchronizing signal at a start of a next successive line of data, whereby for each line of data, the selection of video data is completed during the horizontal synchronizing period following that line of data.

Dependent Claim 2

As recited in Claim 2, the selection device of the format conversion circuit includes a counter (104 of Fig. 8), reset in response to the synchronizing signal detected by said synchronous timing detector, for counting the amount of packet header output from said header generation device

and the amount of video data read out of said memory, and a switch (105 of Fig. 8), which selects the packet header generated by said header generation device until the amount of packet header counted by said counter reaches a predetermined amount, and selects the video data read out of said memory after the amount of packet header counted by said counter has reached the predetermined amount.

Independent Claim 3

Independent Claim 3 recites a format conversion circuit (100 of Fig. 8) for converting the format of digitized video data comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, to a pseudo MPEG2-TS format.

The format conversion circuit comprises a FIFO memory (101 of Fig. 8) for storing the video data in response to a clock for the video data; a header generation circuit (102 of Fig. 8) for generating an MPEG2-TS packet header in response to the clock for the video data; a synchronous timing detection circuit (103 of Fig. 8) for detecting a horizontal synchronizing signal for the video data said horizontal synchronizing signal indicating the end of a

horizontal synchronizing period for a preceding line of data and the start of a next successive line of data; a counter (104 of Fig. 8), reset in response to the horizontal synchronizing signal detected by said synchronous timing detection circuit, for counting the number of bytes of packet header output from said header generation circuit and the number of bytes of video data read out of said FIFO memory; and a switch (105 of Fig. 8), which selects the packet header generated by said header generation circuit until the number of bytes counted by said counter reaches the number of bytes of packet header as specified by MPEG2-TS, and selects the video data read out of said FIFO memory after the number of bytes counted by said counter has reached the number of bytes of packet header as specified by MPEG2-TS, whereby the switch alternately selects the packet header and the video data for successive packets until all video data for a line has been packetized and whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data.

Dependent Claim 4

The invention as set forth in Claim 4 further includes the feature that the counter outputs a data valid signal (page 10, lines 25-28 and page 11, lines 12-13) that indicates the validity of the data, the format of which has been converted to the pseudo MPEG2-TS format, while counting the number of bytes of packet header and the number of bytes of video data.

Dependent Claim 5

The invention as set forth in Claim 5 further includes the feature that the FIFO memory is reset in response to the data valid signal output from said counter to erase the video data stored (page 11, lines 18-20).

VI. GROUND OF REJECTION TO BE REVIEWED

The grounds of rejection in the Final Office Action is that Claims 1-7 have been rejected under 35 USC 103(a) as

being unpatentable over U. S. Patent 6,233,253 of Settle, et al (hereinafter "Settle") in view of U.S. Patent 6,297,794 of Tsubouchi (hereinafter "Tsubouchi") and further in view of U.S. Patent 5,983,237 of Yamauchi (hereinafter "Yamauchi").

VII. ARGUMENT

Claims 1, 6 and 7

35 USC 103(a) as unpatentable over Settle in view of Tsubouchi and Yamauchi

The Settle patent is directed to a system and method for merging and converting digital data received in different formats from different sources into a selected output data format for transmission on a selected transmission channel (see: Abstract). Settle receives input data from multiple sources in the form of packetized digital data (Col. 1, lines 31-32) and demultiplexes the streams, removing header information (Col. 3, lines 41-46). Settle re-formats the packets that contain no header (Col. 3, lines 24-26 and lines 47-49) into MPEG compatible transport packet

form (Col. 3, lines 25-26 and lines 48-49) and adds new headers (Col. 3, lines 27-28 and lines 51-52). Settle multiplexes the re-formatted packets (Col. 3, lines 62-63) to form a new transport stream.

Settle is cited for its teachings regarding generating a packet header. Appellants are aware of the fact that generating packet headers is known. However, what Appellants are claiming includes steps and means for storing unpacketized digitized data, generating a packet header, detecting a synchronizing signal and then alternately repeating the generation of a packet header and selecting a predetermined amount of the video data as a payload responsive to a generated packet header, during an interval between detection of a synchronization signal for a line of data and detection of a synchronization signal for a successive line of data whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data.

The Examiner has concluded that "[r]egarding the 'selection of a predetermined amount of video data of said memory as a payload responsive to the packet header' in claims 1, 6 and 7, Settle et al. produces MPEG-2 transport stream packets (column 4, lines 39-42), which were known to

have a fixed length of 188 bytes each, comprising the packet header and packet payload data." Appellants respectfully contend that Settle does not teach that MPEG-2 packets be produced. Rather, Settle expressly states that it "forms MPEG compatible packets" (Col. 4, line 49) and Settle makes no mention of a fixed packet length. Appellants have contended that Settles teachings regarding packetizing data and generating new headers do not teach the features of the invention as claimed.

The Examiner has acknowledged that Settle does not disclose the storing of unpacketized digitized data, received from a video encoder, in a memory; the detecting of a synchronizing signal; or, the selection of a predetermined amount of video data read out of the memory as a payload responsive to the packet header during an interval between synchronizing signals. The Examiner has further stated on page 4 of the Office Action that "[a]lthough in the header generating device of Settle et al. clock references are periodically added to the resultant multiplexed transport stream...this information is used to synchronize audio and video data at a decoding step, not at encoding, and so does not correspond with the claimed 'synchronizing signal'."

The Examiner has cited the Tsubouchi patent as providing teachings which are missing from the Settle patent. The Tsubouchi reference is directed to a system for displaying requested video content with minimal delay. Tsubouchi provides a dedicated audio-video (AV) bus (4 of Fig. 1) on which a plurality or video devices can deliver video content without going through the system PCI bus (2 of Fig. 1) (see: Abstract and Col. 2, lines 32-42). Tsubouchi minimizes delay by allowing the video devices to directly output the video content to the AV bus. Tsubouchi teaches that it is necessary to enable only one video device at a time to use the AV bus to avoid data collisions (Col. 2, lines 44-51). Tsubouchi teaches six (6) alternative embodiments for switching among video devices to ensure exclusive use of the AV bus, including the use of video output buffers to hold the data to be output until an enable signal enables the output buffer to output the data (Col. 2, lines 55-67).

The Examiner cites the Tsubouchi patent for teaching "that it was known to store video in a buffer, and only read out from the buffer in response to an enable signal." Appellants acknowledge that Tsubouchi teaches that it is known to store video in a buffer and to read the video data out of the buffer in response to a signal.

Appellants maintain however that, even if one having skill in the art were motivated to modify Settle to include the enable-signal-activated buffers of Tsubouchi, one would not arrive at the present invention, since neither Settle nor Tsubouchi teaches or suggests storing video data which has been digitized (i.e., converted in a video encoder from analog format to digital format). Further, neither Settle nor Tsubouchi teaches or suggests that the input video data comprises a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data. Neither Settle nor Tsubouchi teaches detecting a synchronization signal for a line of the video data and packetizing the video data by alternately generating a packet header and selecting a predetermined amount of the video data as a payload until all of the data from the line of video data is packetized. Tsubouchi teaches that an enable signal may be received to allow a device to output video data on the AV bus. However, Tsubouchi does not teach or suggest that the enable signal is a synchronization signal. Finally, neither Settle nor Tsubouchi teaches or suggests the claimed packetizing during an interval between detection of a synchronization signal for the line of data and detection of

a synchronization signal for a successive line of data whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data.

The Examiner acknowledges that "the combination of Settle et al alone *(sic)* and Tsubouchi et al. the *(sic)* enable pulse in Tsubouchi et al. for reading video data from a buffer is not a horizontal synchronization signal, operating on digitized video data comprising a plurality of data lines, each followed by a horizontal synchronization period". The Examiner cites the Yamauchi patent for its teaching of producing a clock signal locked to the horizontal synchronization signal included with video input. As taught by Yamauchi in the Abstract, a "PLL produces a second clock signal based on the vertical synchronization signal included in the video signal" and a "read controller controls the video memory to read out the stored digitized video signal therefrom based on the second control signal". Clearly, Yamauchi is teaching that a read signal is produced based on the vertical synchronization signal, and not on a horizontal synchronization. Yamauchi further states, in Col. 6, lines 11-15, that the read controller receives the

low speech clock signal and fourth reference signal that have been derived from the second and third vertical reference signals (Col. 6, lines 3-10).

The Examiner cites the Yamauchi teachings that digital video is stored into memory based on write signal Sw, citing Col. 5, lines 19-24. The cited teachings are for writing video data into memory using Sf1, a horizontal reference signal for counting samples 123 to 842. Reading out video data, however, is not taught in the cited passage-but is taught in the passages from Col. 6 that are discussed above. The Examiner additionally cites the teaching in Col. 8, lines 1-49. In that cited passage, Yamauchi expressly states that the "low speed PLL 15 produces the low speed clock signal Sc2 synchronized with the V.sync. signal of the input video signal Sv" (Col. 8, lines 23-25) and further that "[b]y using the low speed clock signal Sc2, the stored data is read out from the memory 6" (Col. 8, lines 27-29). Clearly the Yamauchi patent is not teaching the features of the pending claims. Appellants respectfully assert that the presently pending claims do not claim writing video data into the memory in response to a signal. The claims recite steps and means for reading a predetermined amount of video

data out of memory in response to detection of a synchronizing signal for the line of data until detection of a synchronizing signal for a next successive line of data.

Appellants respectfully assert that none of Settle, Tsubouchi or Yamauchi teaches or suggests the claim feature of selection of a predetermined amount of video data during an interval between successively detected synchronizing signals. While Tsubouchi teaches releasing video in response to a signal, Tsubouchi does not teach or suggest releasing a predetermined amount of video during an interval between successive synchronizing signals. While Yamauchi teaches producing a clock signal locked to the horizontal synchronization signal included in video input, there is no teaching or suggestion in Yamauchi, or in the other cited patents, to select or output an amount of data in response to detection of successive synchronizing signals for lines of input data.

For a determination of obviousness, the prior art must teach or suggest all of the claim limitations. "All words in a claim must be considered in judging the patentability of that claim against the prior art" (In re Wilson, 424 F. 2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). A *prima facie* case of obviousness is established when the

teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). A proper *prima facie* case of obviousness cannot be established by combining the teachings of the prior art absent some teaching, incentive, or suggestion supporting the combination. In re Napier, 55 F.3d 610, 613, 34 U.S.P.Q.2d 1782, 1784 (Fed. Cir. 1995); In re Bond, 910 F.2d 831, 834, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990). Appellants conclude that the Examiner has not established a *prima facie* case of obviousness against the pending claims since the combined teachings of Settle, Tsubouchi and Yamauchi do not teach or suggest the claim features of storing video data which has been digitized (i.e., converted in a video encoder from analog format to digital format); detecting a synchronization signal for a line of the video data and packetizing the video data by alternately generating a packet header and selecting a predetermined amount of the video data as a payload until all of the data from the line of video data is packetized, between detection of a synchronization signal for the line of data and detection of a synchronization signal for a successive line of data whereby, for each line of data, the selecting of

video data is completed during the horizontal synchronizing period following that line of data. Appellants conclude that the Examiner has not established a *prima facie* case of obviousness against Claims 1, 6 and 7 and should be overturned.

Claim 2

Claim 2 recites all of the limitations of Claim 1,and Appellants rely on the arguments set forth above with respect to those claim features. Claim 2 also expressly recites a counter, reset in response to the synchronizing signal detected by said synchronous timing detector, for counting the amount of packet header output from said header generation device and the amount of video data read out of said memory, and a switch, which selects the packet header generated by said header generation device until the amount of packet header counted by said counter reaches a predetermined amount, and selects the video data read out of said memory after the amount of packet header counted by said counter has reached the predetermined amount. The Examiner concludes that "since Settle et al. is an MPEG-2 transport system encoder, it is inherent that it includes counters for counting packet header length and total packet length, and a *selector* to output payload data after a packet header has concluded, to produce valid MPEG-2 transport stream packets" (emphasis added). Appellants are not claiming a selector in Claim 2. Moreover, Appellants

reiterate that Settle teaches "MPEG compatible system transport packets" (Col. 4, line 54) and further that Settle does not teach or suggest a predefined packet length. Moreover, Settle does not teach or suggest a counter and switch. The Examiner concludes that it would be inherent that Settle includes a counter and selector. Since Settle does not teach a predefined packet length, and is only producing "MPEG compatible" packets, it cannot be concluded that Settle inherently includes a counter and switch as claimed.

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record." (In re Lee, 277 F. 3d 1338, 1343 (Fed. Cir. 2002)). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority" (Id. at 1343-1344). "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." In re Kahn, 441 F.3d 977,

988, 78 USPQ2d 1329, 1336, quoted with approval in KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007). Since the Examiner does not point to express teachings, and cannot rely on conclusory statements on inherency, Appellants believe that a *prima facie* case of obviousness has not been sustained with respect to Claim 2 and that the rejection should be overturned.

Claim 3

Claim 3 parallels Claim 2, with the features of Claim 1, but additionally expressly recites a format conversion circuit for converting the format of digitized video data to MPEG2-TS format. Appellants rely on the arguments set forth above with respect to the claim features of Claims 1 and 2. Moreover, Appellants disagree with the Examiner's conclusion that "Settle, et al. outputs video data as MPEG-2 transport stream packets". As discussed above, Settle only teaches that MPEG compatible packets be produced. The Examiner further concludes that "video capture 31 of Tsubouchi et al. contains an output buffer for outputting video to a dedicated bus (column 2:lines 55-57) corresponding with the FIFO memory." Appellants respectfully disagree. The FIFO

memory as recited in Claim 3 is "a FIFO memory for storing the video data in response to a clock for the video data". Tsubouchi does not teach or suggest a FIFO for storing data in response to a clock for the video data. In the cited passage, Tsubouchi simply teaches that each video device has an output buffer with means for enabling or disabling the output buffer to output the data. Tsubouchi does not teach or suggest a FIFO and does not teach that the output buffer stores data in response to a clock for the video data. Clearly the combination of teachings does not obviate the language of Claim 3.

Claim 4

Claim 4 recites all of the limitations of Claim 3 and additionally recites the counter counting and outputting a data valid signal (Claim 4). Appellants rely on the arguments set forth above with respect to the features already discussed. The Examiner cites Yamauchi against Claim 4 stating that Yamauchi teaches in Col. 5, lines 17-26 that the video write signal Sw is only enabled during the period in a particular line of video when the converted video signal corresponds to effective video data.

Appellants reiterate that the cited Yamauchi's teachings relate to writing data into a video memory and not to a counter outputting a data validity signal while counting bytes of header and video data. Moreover, writing only valid data into a memory location is not the same as or suggestive of generating a data validity signal along with output video data being read from FIFO memory. Clearly the Examiner has not established a *prima facie* case of obviousness against the language of Claim 4 and reversal of the rejection is respectfully requested.

Claim 5

Claim 5 recites all of the limitations of Claim 4 and additionally recites that the FIFO memory is rest in response to the data valid signal output from the counter to erase the stored video data. Appellants rely on the arguments set forth above with respect to the features already discussed. Appellants further argue that the Examiner has again erred in citing the video data writing teachings of Yamauchi against the claim language. As detailed above, Yamauchi's teachings regarding writing video

data into memory are not germane to the claim features regarding reading video data out of memory.

The Examiner acknowledges that Yamauchi does not disclose "producing a data valid signal based on a horizontal synchronization signal from a memory write controller instead of a packet header length counter." Appellants note that the same conclusion should have been incorporated into the Examiner's remarks when rejecting Claim 4. Appellants believe that the Examiner's acknowledgment undermines the rejection of Claim 4 above and further supports Appellants conclusion that the rejection was erroneous.

With respect to this acknowledgment in the rejection of Claim 5, Appellants agree that Yamauchi fails to disclose that feature. Appellants disagree with the Examiner's subsequent statement that "the 'data valid signal' in claims 4 and 5 is considered equivalent under the Doctrine of Equivalents to the 'writing signal' in Yamauchi et al. since...the signal performs the same function...in substantially the same way...to produce substantially the same result". The data valid signal of the present invention is not a write signal, and is not even a read

signal. The data valid signal is an indicator that video data has been successfully read out of the memory. Once the data valid signal has been generated, the FIFO memory can be reset to erase the stored video data, since that video data has been successfully read and need not be stored any longer. The data valid signal is ***not*** a write signal and does not perform the same function as a write signal. In fact, the function of the data valid signal to notify the memory that it can erase the stored video data effectively performs the ***exact opposite*** function of that performed by a write signal. Clearly the Examiner's conclusions regarding the applicability of the Yamauchi teachings to the claim language cannot be sustained. Accordingly, Appellants request reversal of the rejection of Claim 5.

CONCLUSION

Appellants respectfully assert that the Examiner has erred in rejecting Claims 1-7 as unpatentable over Settle in view of Tsubouchi and Yamauchi. Appellants request that the decisions of the Examiner be overturned by the Board and that the claims be passed to issuance.

Respectfully submitted,

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APPENDIX OF CLAIMS

1. A format conversion circuit for conversion of digitized video data comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, comprising:

a memory for storing video data;

header generation device for generating a packet header that adheres to a standard for motion picture compression;

synchronous timing detector for detecting a synchronizing signal for a line of video data; and

selection device for repeating the selection of the packet header generated by said header generation means and selection of a predetermined amount of video data read out of said memory as a payload responsive to the packet header, during an interval from when said synchronous timing detection device detects the synchronizing signal for the line of data until it detects the next synchronizing signal at a start of a next successive line of data,

whereby for each line of data, the selection of video data is completed during the horizontal synchronizing period following that line of data.

2. A format conversion circuit according to claim 1, wherein said selection device includes

a counter, reset in response to the synchronizing signal detected by said synchronous timing detector, for counting the amount of packet header output from said header generation device and the amount of video data read out of said memory, and

a switch, which selects the packet header generated by said header generation device until the amount of packet header counted by said counter reaches a predetermined amount, and selects the video data read out of said memory after the amount of packet header counted by said counter has reached the predetermined amount.

3. A format conversion circuit for converting the format of digitized video data comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, to a pseudo MPEG2-TS format, comprising:

a FIFO memory for storing the video data in response to a clock for the video data;

a header generation circuit for generating an MPEG2-TS packet header in response to the clock for the video data;

a synchronous timing detection circuit for detecting a horizontal synchronizing signal for the video data said horizontal synchronizing signal indicating the end of a horizontal synchronizing period for a preceding line of data and the start of a next successive line of data;

a counter, reset in response to the horizontal synchronizing signal detected by said synchronous timing detection circuit, for counting the number of bytes of packet header output from said header generation circuit and the number of bytes of video data read out of said FIFO memory; and

a switch, which selects the packet header generated by said header generation circuit until the number of bytes counted by said counter reaches the number of bytes of packet header as specified by MPEG2-TS, and selects the video data read out of said FIFO memory after the number of bytes counted by said counter has reached the number of bytes of packet header as specified by MPEG2-TS,

whereby the switch alternately selects the packet header and the video data for successive packets until all video data for a line has been packetized and whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data.

4. A format conversion circuit according to claim 3, wherein said counter outputs a data valid signal that indicates the validity of the data, the format of which has been converted to the pseudo MPEG2-TS format, while counting the number of bytes of packet header and the number of bytes of video data.

5. A format conversion circuit according to claim 4, wherein said FIFO memory is reset in response to the data valid signal output from said counter to erase the video data stored.

6. A method for converting the format of digitized video data comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, said method comprising:

storing video data;

generating a packet header that adheres to a standard for motion picture compression;

detecting a synchronization signal for a line of the video data; and

repeating the generation of a packet header and selecting a predetermined amount of the video data as a payload responsive to latter said packet header, during an interval between detection of a synchronization signal for the line of data and detection of a synchronization signal for a successive line of data whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data.

7. A computer readable storage device encoded with a computer program readable by a digital processing apparatus and having a program of instructions which are tangibly embodied on the storage device and which are executable by the processing apparatus to perform a method of converting the format of digitized video data comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, said method comprising:

storing video data;

generating a packet header that adheres to a standard for motion picture compression;

detecting a synchronization signal for a line of the video data; and

repeating the generation of a packet header and selecting a predetermined amount of the video data as a payload responsive to latter said packet header, during an interval between detection of a synchronization signal for the line of data and detection of a synchronization signal for a successive line of data whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data.

EVIDENCE APPENDIX

There is no additional evidence.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.